

Abstract of the Disclosure

A clock signal generator having first and second coarse delay circuits connected in series delays pulses of a reference signal having period  $T_p$  to produce pulses of the clock signal. The first coarse delay circuit delays pulses of the reference signal with a delay resolution of  $T_p/N$  seconds over a range spanning  $T_p$  seconds to produce pulses of an output signal. The second coarse delay circuit delays pulses of the output signal of the first coarse delay circuit over a range spanning  $T_p$  seconds with a delay resolution of  $T_p/M$  seconds to provide pulses of the clock signal with a timing resolution of  $T_p/(M*N)$  seconds when the integers  $N$  and  $M$  are relatively prime.